Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **D1**
2. **N/C**
3. **D3**
4. **S3**
5. **S4**
6. **D4**
7. **N/C**
8. **D2**
9. **S2**
10. **IN2**
11. **V+**
12. **VL**
13. **VR**
14. **V-**
15. **IN1**
16. **S1**

**.080”**

**7\*011**

**B 1**

**CMJV**

**.044”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 89226**

**APPROVED BY: DK DIE SIZE .044” X .080” DATE: 10/13/21**

**MFG: SILICONIX THICKNESS .015” P/N: DG189/DG190/DG191**

**DG 10.1.2**

#### Rev B, 7/1